Applicants:	Walter Fix et al.
Serial No.:	10/562,869
Filed:	April 7, 2006
For:	Logic Gate with a Potential-Free Gate Electrode for Organic Integrated Circuits
Examiner:	Eva Y. Montalvo Art Unit: 2814
Attorney Dkt:	411000-144 Customer No. 27162

PETITION TO WITHDRAW FINALITY OF ACTION UNDER 37 CFR 1.181

MS Amendment
Commissioner for Patents
Box 1450
Alexandria, VA 22313-1450

This is a petition to invoke the supervisory authority of the Director to withdraw the finality of the Office Action dated 12/28/09 in the above entitled application. While no fee is believed due for this paper, the Commissioner is authorized to charge deposit account 03 0678 for any fee that might be due for this paper.

In the prior Office Action dated 6/24/09, claim 1 is rejected under 35 USC 112, 1st paragraph (new matter) as presented below prior to the amendment made below regarding the "switching" term. In addition, the term "input" is objected to as not having antecedent basis. Accordingly, claim 1 was amended in response to the 6/24/09 Action as set forth below. This amendment plainly was made to meet formal objections to the prior claim 1 and does not include any substantive changes to overcome any art of record.

The term input is added at line 2 as required and the terms "switching" is changed to "charging" to correct a prior error made in this claim. The "switching" terms were inadvertently added to replace the "charging" terms in a prior amendment.

The claim as amended below was present in a response filed 8/11/08 to an Office Action dated 5/14/08. The below claim 1 (as existed after the amendment made below) was acted upon in a prior Final Action dated 12/16/08 in which a reference is cited against this claim 1. This reference is different than the reference now being cited in the present final Action.

Applicants responded to the 12/16/08 Action with an RCE and a response after final and a supplemental response, the latter being filed on 4/15/09. The latter response inadvertently amended claim 1 in error as noted above changing the "charging" term to "switching", which error is corrected by claim 1 presented below in response to the formal matter rejection under 35 USC 112 in the 12/28/09 Office Action.

Therefore, there are no new issues presented to the Office by the below claim 1 warranting a new further search and the issuance of the Final Action objected to by this petition. Since the amendment below is made to meet formal objections only, and since this claim was acted upon by the Office in a prior Action, the finality of the Action of 12/28/09 is premature and should be withdrawn.

The undersigned had an interview with the Examiner and her supervisor on Jan. 27, 2010 in regard to this and other matters. They refused to withdraw the finality, as requested by the undersigned during the interview.

Since there are no new issues in this application and the amendment to claim 1 below was made only to meet formal objections in a prior Action, and was previously acted upon by the Office, the finality of the Action of 12/28/09 should be withdrawn.

1. An organic logic gate comprising:
a circuit having an input and an output and comprising at least one organic charging field effect transistor (charging FET) on a substrate;
the charging FET including a first structured layer comprising source and drain electrodes;
followed by a semiconductor layer on the electrodes followed by a layer of insulating material on the semiconductor layer and adjacent to and contiguous with a second electrode layer forming a gate electrode; and
at least one switching organic field effect transistor (switching FET) having at least one gate electrode, a source electrode and a drain electrode;
the drain-source electrodes of the charging and switching transistors being arranged to be coupled in series between a voltage source and a reference potential such that the gate electrode of the charging FET is not connected via an electrical line directly to a voltage source, to the reference potential, to the input or to the output;
wherein the gate electrode of the charging ~~switching~~ FET is directly capacitively coupled to one of the source/drain electrodes of the charging ~~switching~~ FET.

The Commissioner is authorized to respectively charge or credit deposit account 03 0678 for any under or overpayments in connection with this paper as noted on the first page of this paper.

Respectfully submitted,
Walter Fix et al.

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